UM10063

ISP1506 ULPI transceiver eval board, supporting Hi-Speed USB host, peripheral and OTG

Rev. 01 — 7 July 2006 User manual

Document information

Info	Content
Keywords	isp1506, usb, ulpi, universal serial bus, transceiver, utmi+ low-pin interface, host, peripheral, otg
Abstract	The ISP1506 ULPI transceiver evaluation (eval) board allows you to evaluate the features of the ISP1506. This document describes the eval board.

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Revision history

Rev	Date	Description
01	20060707	First release.

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1. Introduction

The ISP1506 is a 4-bit bidirectional UTMI+ Low Pin Interface (ULPI) transceiver, which provides a Hi-Speed Universal Serial Bus (USB) analog front-end solution to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) to implement as a Hi-Speed USB host, peripheral or OTG device.

The ISP1506 evaluation (eval) board allows you to evaluate the features of the ISP1506 for performance measurement and functionality characterization. The eval board also allows the ULPI Transceiver and Macrocell Tester (T&MT) interface to be connected to a USB link to validate the transceiver.

Fig 1 shows the ISP1506 eval board.

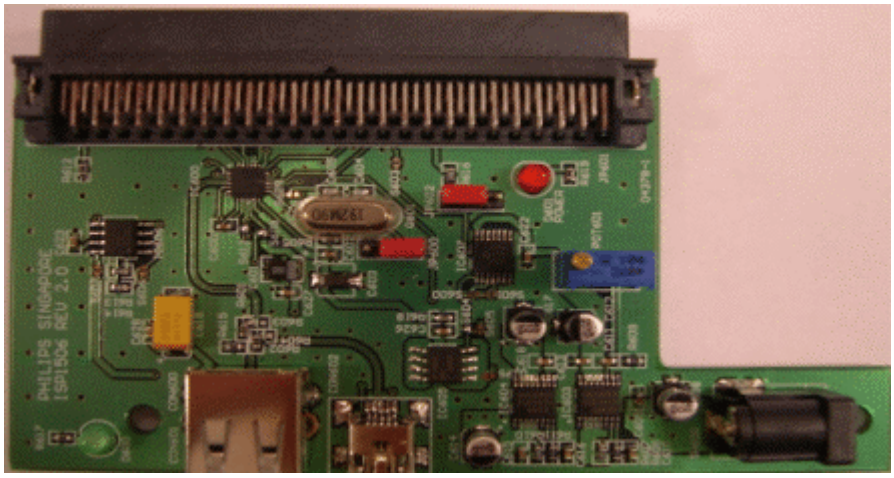

Fig 1. ISP1506 eval board

2. Features

2.1 Functionality

- Fully complies with Universal Serial Bus Specification Rev. 2.0
- On-chip 1.5 kΩ pull-up resistor on DP and 15 kΩ pull-down resistors on DP and DM; optional external 1.5 kΩ low-speed pull-up resistor on DM provided on-board
- On-chip 45 Ω resistors on DP and DM for high-speed termination
- All UTMI+ static signals are accessed using register map
- 60 MHz clock out (4-bit DDR data interface that clocks on both the rising and falling edges of the clock), can be configured to drive 60 MHz from the USB link on the same pin
- Supports full-speed and low-speed UTMI+ serial interface
- Supports high-speed, full-speed and low-speed disconnect detection
- 4-bit DDR data bus that allows USB packet transaction and register access
- Supports UTMI+ OTG interface with an internal 50 mA charge pump, or an external V_{BUS} switch or charge pump; an external solution must be used for V_{BUS} current requirements higher than 50 mA.

2.2 Connectors

- USB connectors: standard-A, standard-B and mini-AB
- ULPI through T&MT connector
- Input power connector.

2.3 Power supplies

- The board power can be directly supplied from an external power supply or from a link through the T&MT connector.
- The V_{BUS} power supply is generated from the on-chip charge pump or from the link through the T&MT connector.

3. Board usage

3.1 ISP1506 daughter card overview

The ISP1506 daughter card is designed to connect to either an ASIC or a generic Field Programmable Gate-Array (FPGA) link board through a 100-pin T&MT connector to provide an interface for system validation. See Fig 2.

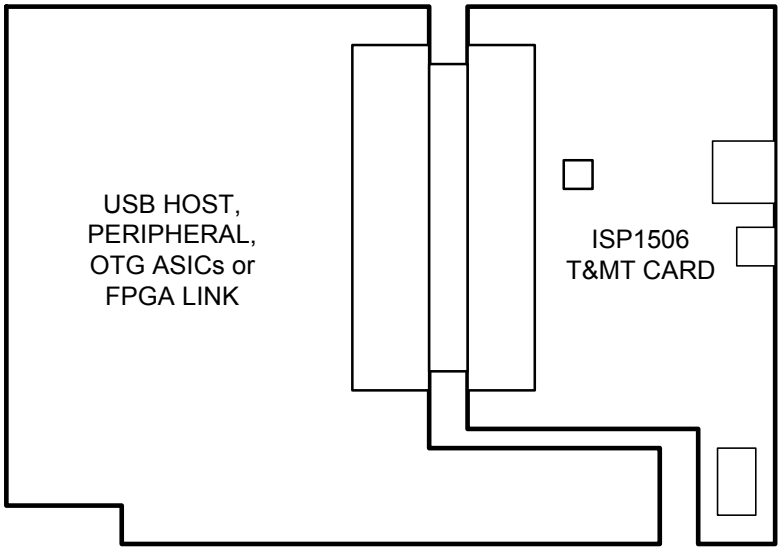

Fig 2. ISP1506 T&MT card with a link

3.2 Block diagram

Fig 3 shows the design overview of the board.

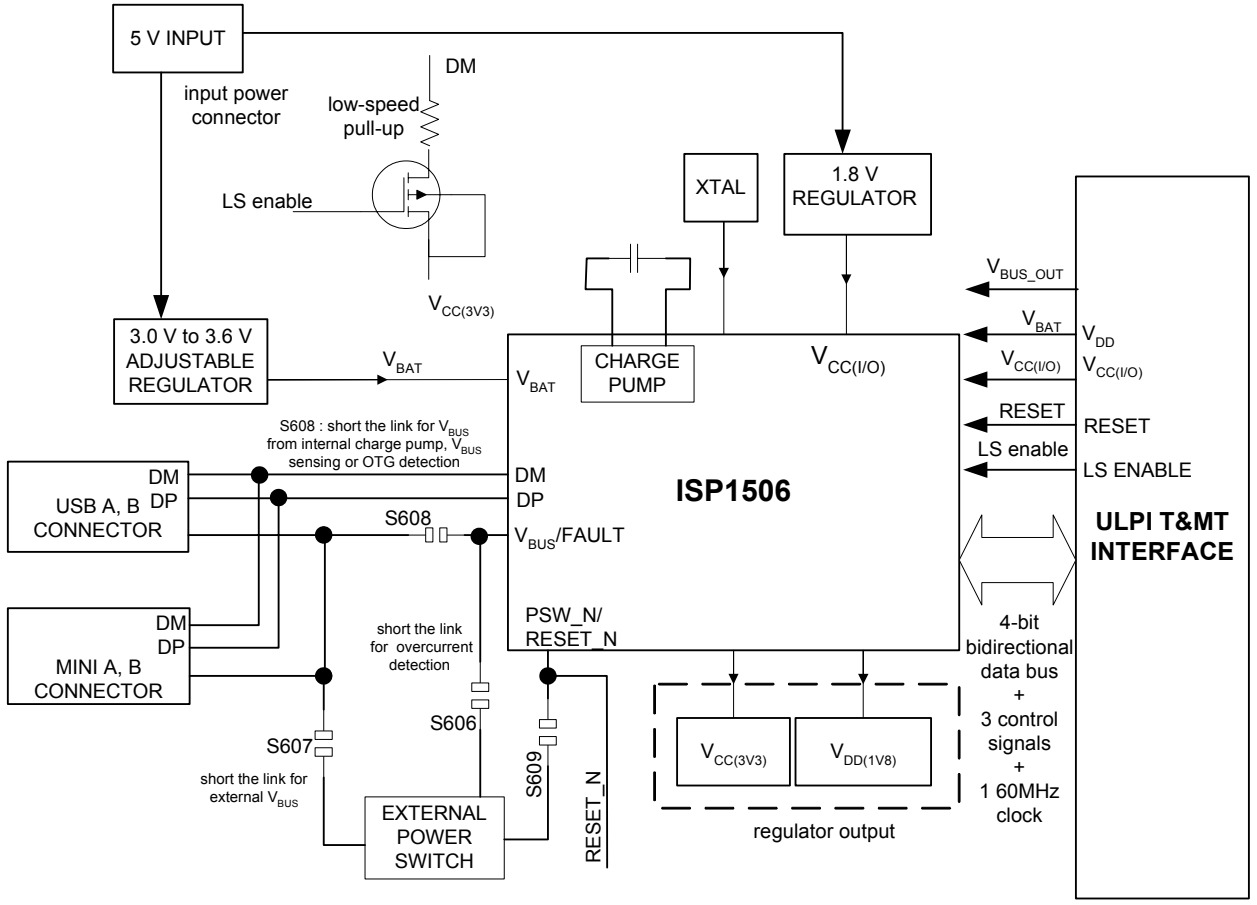

Fig 3. ULPI T&MT card block diagram

4. Eval board usage

4.1 Power supply

The ISP1506 eval board can be powered either through the input power connector (SW600) or through the T&MT connector. If power is supplied from the link, pin 100 of the T&MT connector must be connected to ground on the link side (see Fig 4). This is because once the two boards are connected together; LOW on pin 100 will shut down the regulator outputs from IC603 and IC604 to the ISP1506. If pin 100 is left open, the ISP1506 must be powered through SW600 (see Fig 5).

There are two voltage regulators on the eval board powering V_{BAT} and $V_{CC(I/O)}$. V_{BAT} is powered by an adjustable voltage regulator (IC603), whose output voltage must be set to a voltage between 3.0 V and 3.6 V through trimmer pot POT601. $V_{CC(I/O)}$ is powered by a 1.8 V fixed output voltage regulator (IC604). LED D601 indicates the availability of V_{BAT}.

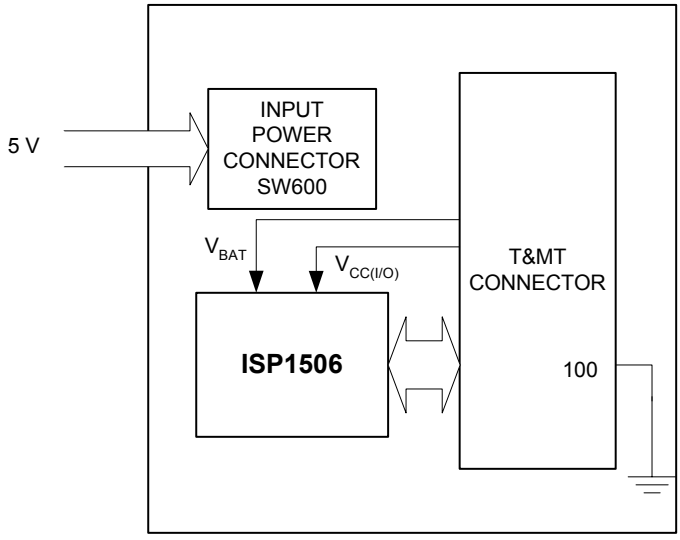

Fig 4. Power supply selection from the T&MT connector

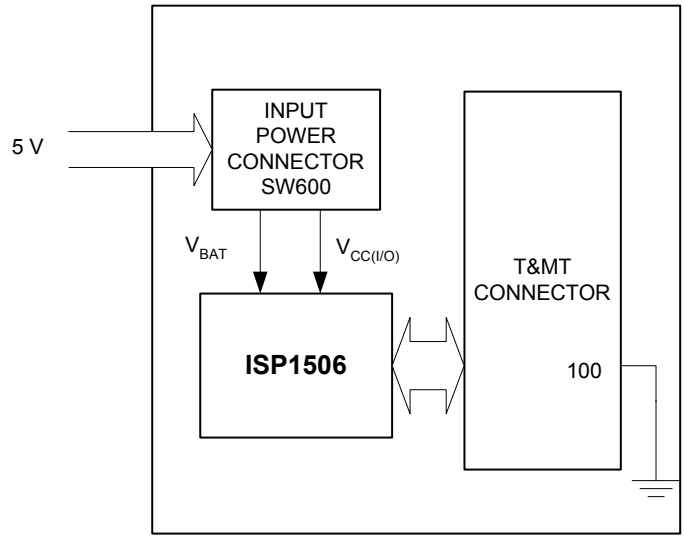

Fig 5. Power supply selection from the on-board regulators

4.2 Using V_{BUS} as a host transceiver

An OTG A-device or a standard USB host provides V_{BUS}. There are two ways V_{BUS} can be driven: from the ISP1506 internal 50 mA charge pump, or from an external V_{BUS} power switch or charge pump that provides higher current drive capability.

4.2.1 V_{BUS} from the ISP1506

The ISP1506 can use its internal charge pump to supply V_{BUS}. To achieve this:

1. Set bit 5 (DRV_VBUS) of the OTG Control register (0Ah) to logic 1.
2. Set bit 6 (DRV_VBUS_EXT) of the OTG Control register (0Ah) to logic 0 (default).

3. Set bit 7 (USE_EXT_VBUS_IND) of the OTG Control register (0Ah) to logic 0 (default).

If using the internal charge pump, short bridge S608 for V_{BUS}; see Fig 6.

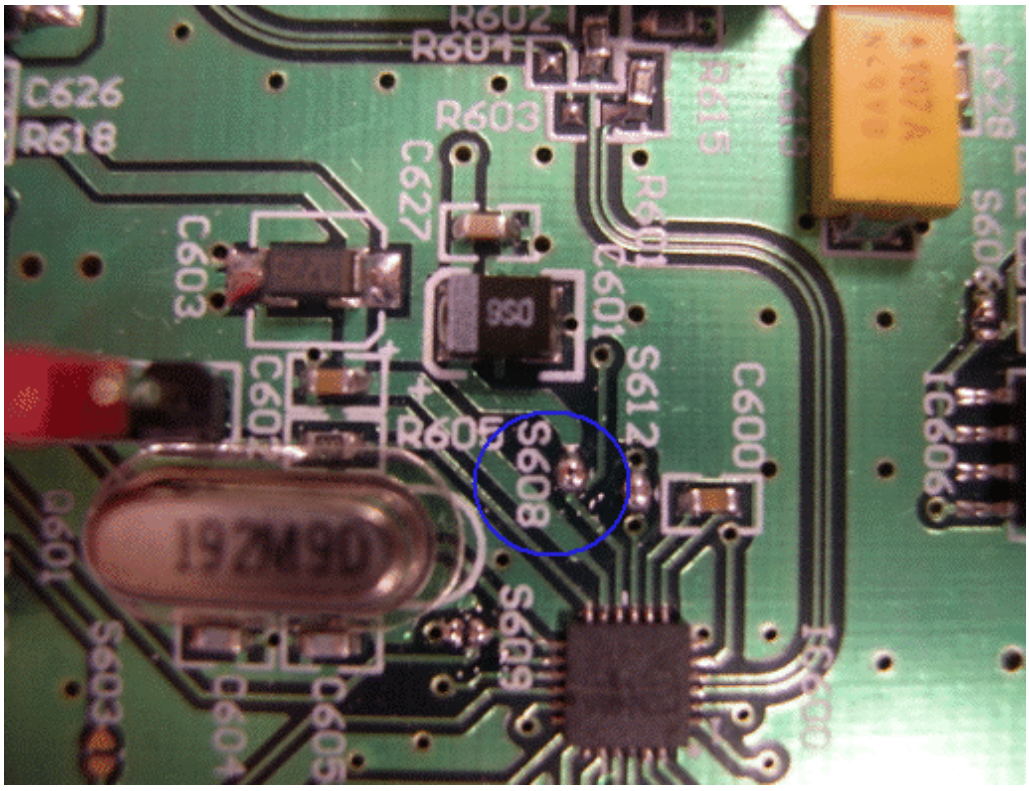

Fig 6. Shorting bridge S608 for V_{BUS} from the internal charge pump

4.2.2 V_{BUS} from an external source

If you want to drive V_{BUS} from an external source, for example, 5 V from the link, you need to:

1. Use the T&MT connector to supply V_{BUS} through pin V_{BUS_OUT} (pin 28 of JP601).
2. Route PSW_N to pin 1 of IC606 by opening S600 and S601 and shorting S609. See Section 4.6.
3. Route the FAULT output pin (pin 2 of IC606) to V_{BUS}/FAULT (pin 10 of IC600) by shorting S606 and opening S608.
4. Short S607 so that V_{BUS} can be directed to CON600 or CON602.
5. Set bit 5 (IND_COMPL) of the Interface Control register (07h) to logic 0 (default).
6. Set bit 6 (IND_PASS_THRU) of the Interface Control register (07h) to logic 1.
7. Set bit 5 (DRV_VBUS) of the OTG Control register (0Ah) to logic 0 (default).
8. Set bit 6 (DRV_VBUS_EXT) of the OTG Control register (0Ah) to logic 1.
9. Set bit 7 (USE_EXT_VBUS_IND) of the OTG Control register (0Ah) to logic 1.

These settings will enable the external V_{BUS} switch. Once the external V_{BUS} switch (IC606) is turned on, the green LED (D600) will light up. For details, see Section 6.

4.2.3 Driving V_{BUS} on USB standard-A connector

If you are evaluating the ISP1506 as a host transceiver, short bridge S602 so that V_{BUS} will be routed to the V_{BUS} pin of the type-A connector (CON600).

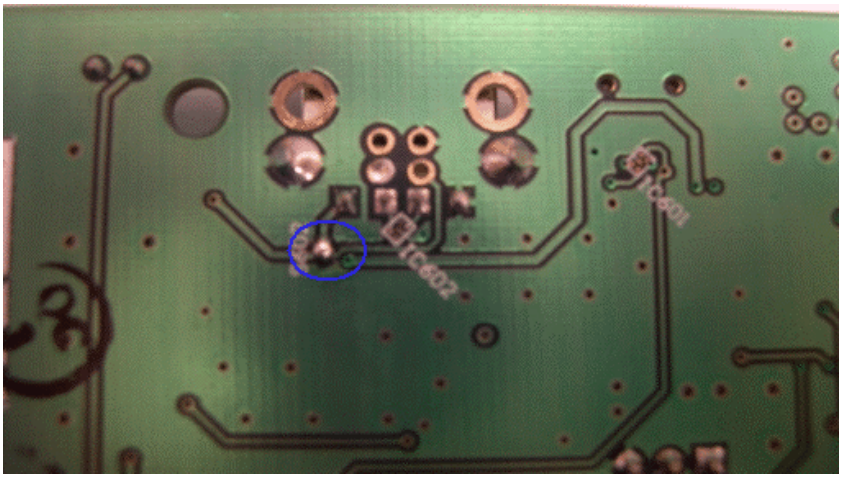

Fig 7. S602

4.3 Using V_{BUS} as a peripheral

If you are evaluating the ISP1506 as a peripheral transceiver, solder bridge S602 must be opened. The transceiver has an internal V_{BUS} comparator that will sense the V_{BUS} voltage level on the V_{BUS} pin (pin 10 of IC600).

4.4 DP and DM lines

There are three types of USB connectors on the ISP1506 eval board: standard-A, standard-B and mini-AB. The footprints of the standard-A and standard-B connectors are placed together; that is, either standard A-or standard-B connector can be mounted on the eval board. The mini-AB connector is placed adjacent to standard-A and standard-B connectors. To have a better control on the impedance of the DP and DM lines, 0 Ω jumper resistors are used to separate the path to the USB type-A or type-B, and the mini-AB connector. Bridge R601 and R602 on the board if you want to send or receive USB packets through the standard-A or standard-B connector (see Fig 8). Bridge R603 and R604 on the eval board if you want to send or receive USB packets through the mini-AB connector.

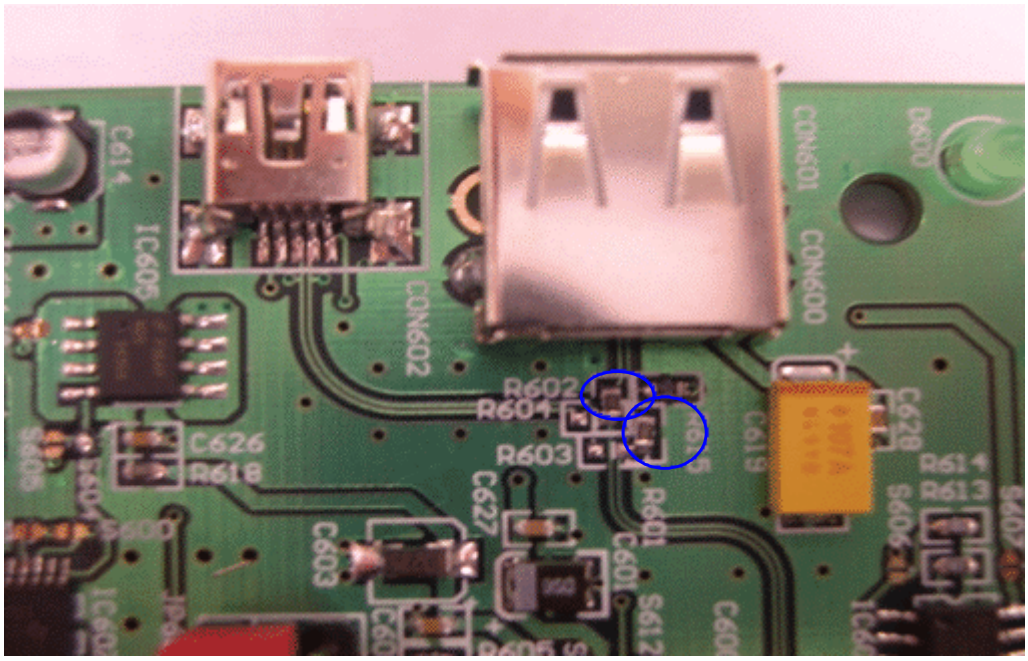

Fig 8. R601 (DM) and R602 (DP)

A summary of the transceiver configuration for various applications is given in Table 1.

Table 1. Summary of the transceiver configuration for various applications

Component	PC host transceiver	PC peripheral transceiver	OTG transceiver (internal charge pump)	OTG transceiver (external charge pump or power switch)
R601	√	√	X	X
R602	√	√	X	X
R603	X	X	√	√
R604	X	X	√	√
S602	√	X	X	X
S606	√	X	X	√
S607	√	X	X	√
S608	X	√	√	X
S609	√	X	X	√
S600	X	X	X	X
S601	X	√	√	X

4.4.1 Pull-up resistor for low-speed only peripheral

The ISP1506 does not provide a pull-up resistor on the DM line for low-speed only peripheral. Therefore, the USB device link must provide a low-speed enable signal to

activate the pull-up resistor on the DM line for a low-speed only peripheral. The low-speed enable signal is located on pin 20 of T&MT connector JP601. It is routed to the switching circuit on the eval board, consisting of R615 and IC605. R615 is a pull-up resistor. The inverter (IC607A) will be required if the low-speed enable is active HIGH because the gate of the PMOS switch must be LOW to route 3.3 V to the pull-up resistor. S604 and S605 provide the flexibility to bypass or use the inverter. Header JP602 allows you to manually control the DM switching, without the low-speed enable.

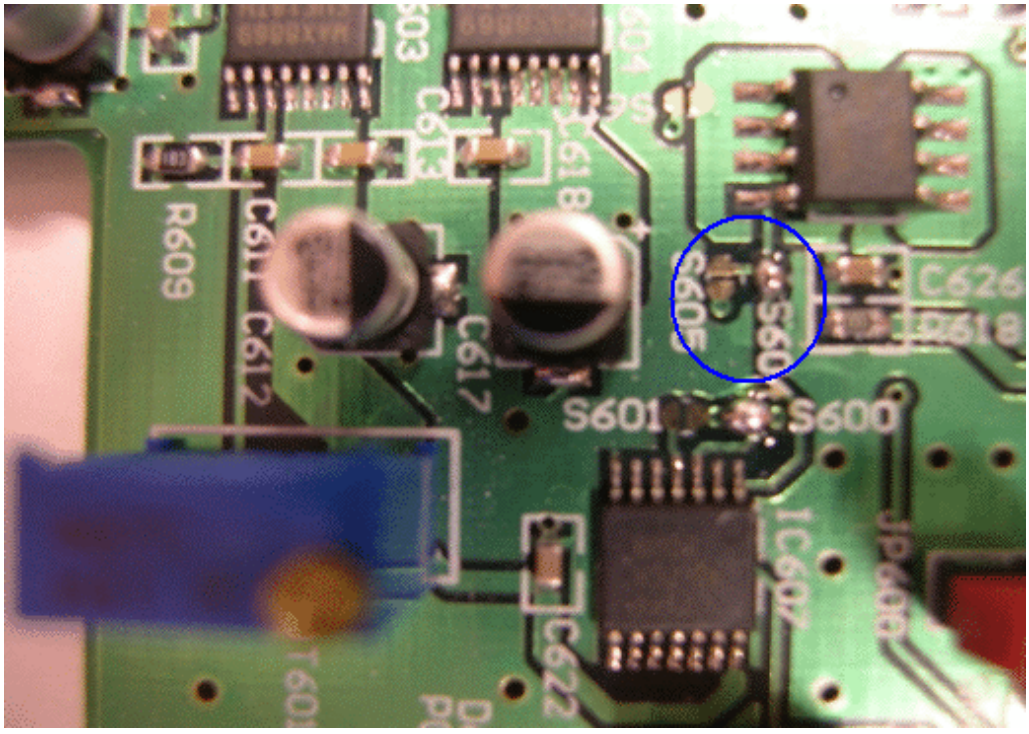

Fig 9. S603, S604, S605 IC607 for low-speed enable

4.5 Clock supply

There are three ways the 60 MHz clock can be supplied:

- Through the crystal oscillator attached between XTAL1 and XTAL2 (pins 12 and 13). The value of the crystal depends on the silicon version. For details, see Section 7.
- Through an external clock driven into the XTAL1 pin by removing the jumper on JP600 and applying an external clock on pin 2 of JP600. The value of the external clock depends on the silicon. For details, see Section 7.
- Through a 60 MHz clock driven into CLOCK (pin 19 of the ISP1506). In this case, the jumper on JP600 must be removed and a DC voltage of 1.8 V must be applied to XTAL1 (REG1V8 regulator output can be connected to the XTAL1 pin).

Fig 10 shows the JP600 header to facilitate the clock selection, without removing the crystal oscillator.

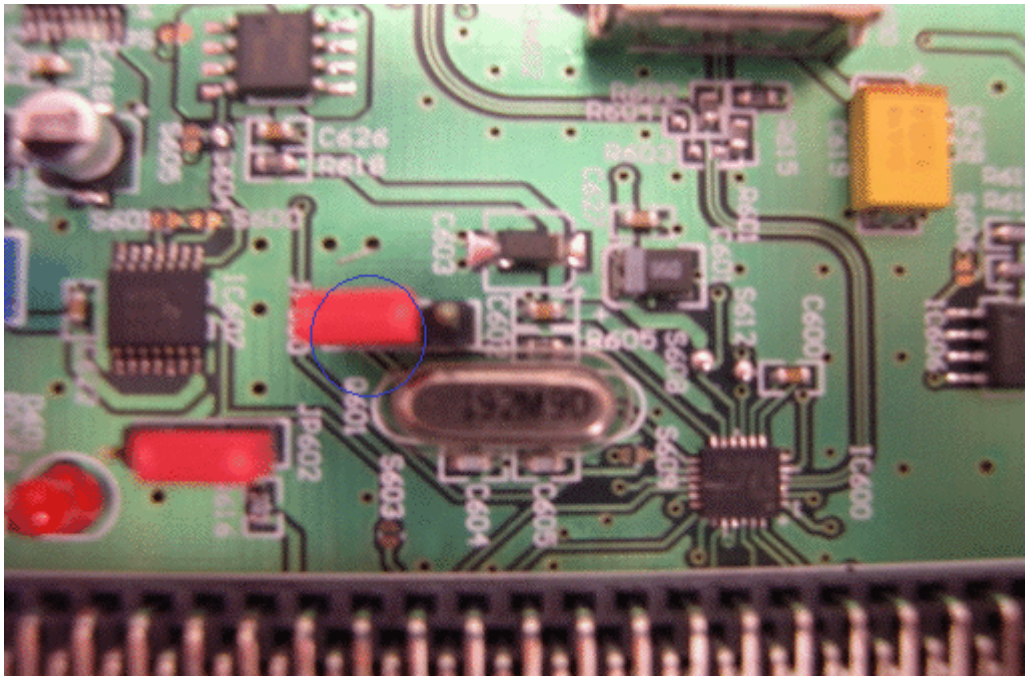

Fig 10. Clock generation: JP600 header

4.6 Reset

The ISP1506 reset is an active LOW asynchronous input that resets all circuitry. The reset pin is multiplexed with PSW_N. If on-board V_{BUS} power switch is used to drive V_{BUS}, short S609. This allows you to bridge PSW_N to the V_{BUS} power switch (IC606). IC607B is an inverter to invert the polarity of reset signal if the reset from the link is active HIGH.

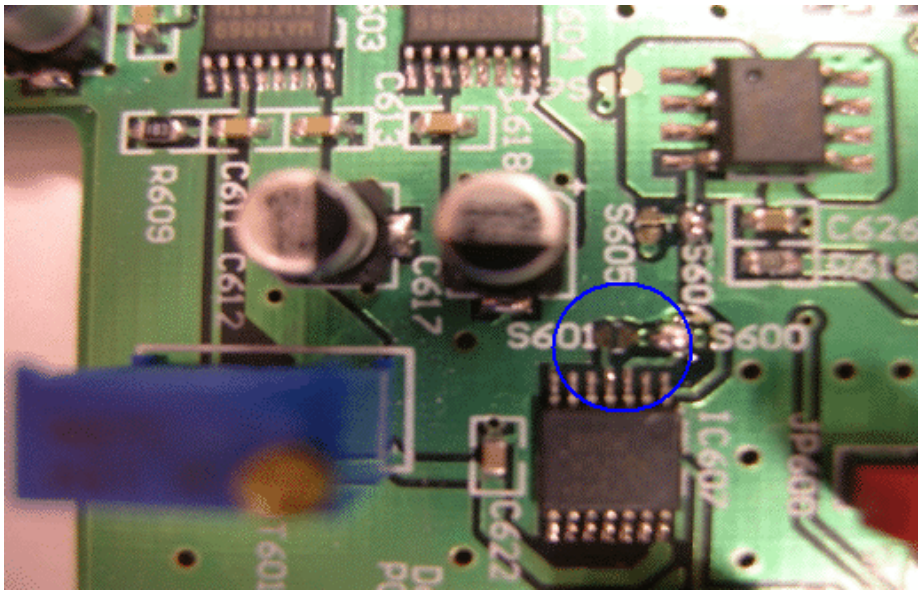

Fig 11. S600, S601 IC607 for reset

5. PCB guidelines

The ISP1506 eval board contains four layers. The top and bottom layers consist of signal, ground and power tracks, while the second and third layers are ground and power planes.

Some guidelines that may be followed when designing a transceiver board are:

- To get stable band gap reference V_{REF}, place the RREF resistor R600 close to pin 2 of IC600. R600 must have a tolerance of 1 % or better.
- The flying capacitor (C600) for the charge pump must be placed close to pin 7 (C_B) and pin 8 (C_A) of IC600.
- Place decoupling capacitors close to the supply pins of the IC. If there is a high-radiated emission, ferrite beads can be used, and must be placed close to supply pins $V_{CC(I/O)}$ and V_{BAT}. The ferrite beads used in the application can be between 50 Ω and 120 Ω at 100 MHz, with current rating of approximately 200 mA.
- Place decoupling capacitors close to the output pins of the 1.8 V and 3.3 V regulators.
- Place the crystal oscillator and the two load capacitors close to XTAL1 and XTAL2 of the IC.
- To achieve a differential impedance of 90 Ω, the trace width and spacing of DP and DM must comply with the *Universal Serial Bus Specification Rev. 2.0* requirement of 7.5 mils width and 7.5 mils spacing. Also, the parallelism of the DP and DM lines must be maintained. Avoid stubs on the lines.
- Ground vias are recommended for ground plane interconnect and must be kept apart by a maximum distance of 10 mm x 10 mm.
- The exposed die pad at the bottom of the ISP1506 is a ground and therefore, must be grounded on the PCB board for the transceiver to function properly.
- Route the clock out away from the data line to avoid crosstalk. It is also recommended that you route ground tracks between the clock traces. If there is high emission on the clock and its harmonics, insert a series resistor on the 60 MHz clock out pin.

6. Schematics

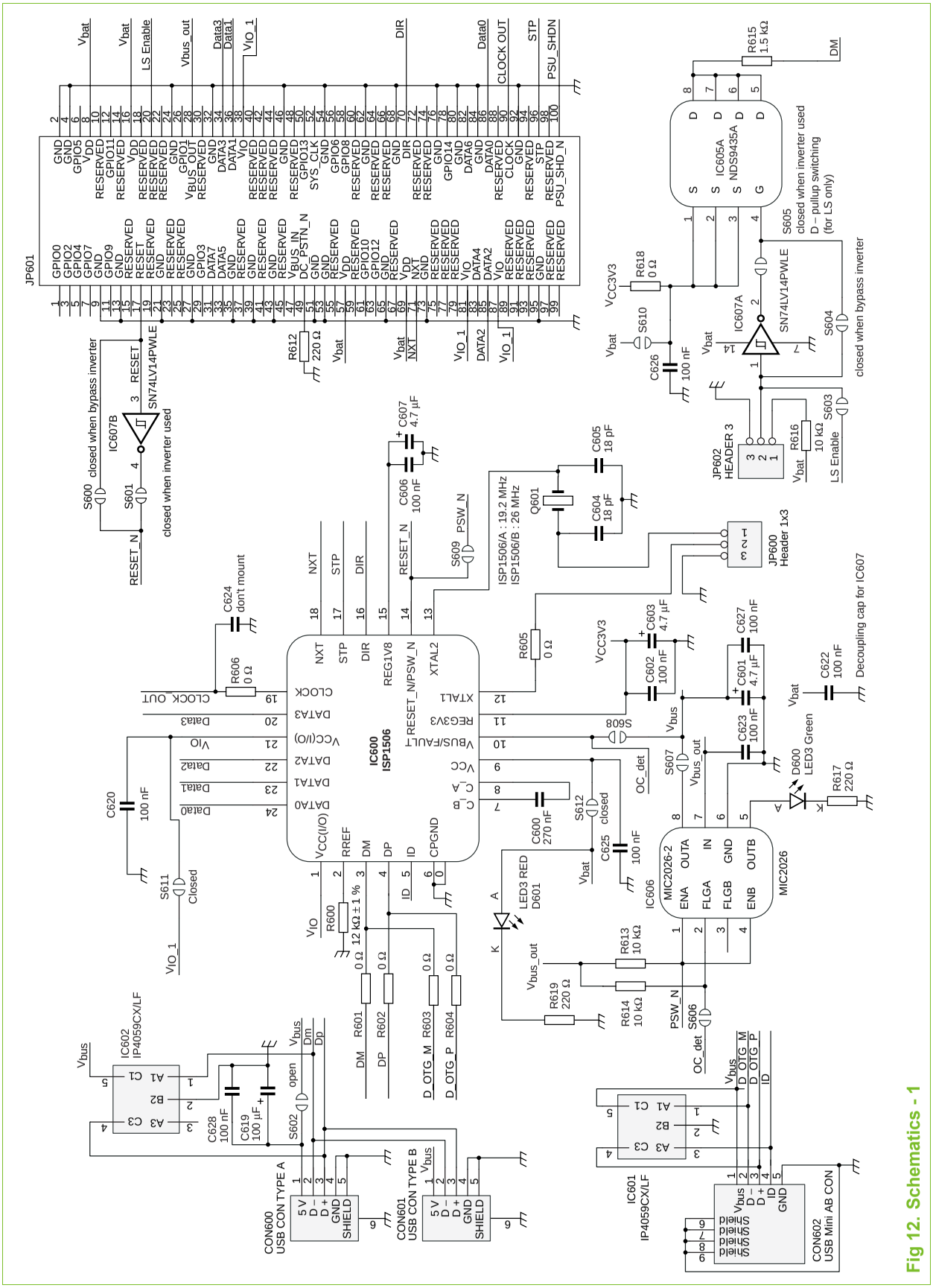

Fig 12. Schematics - 1

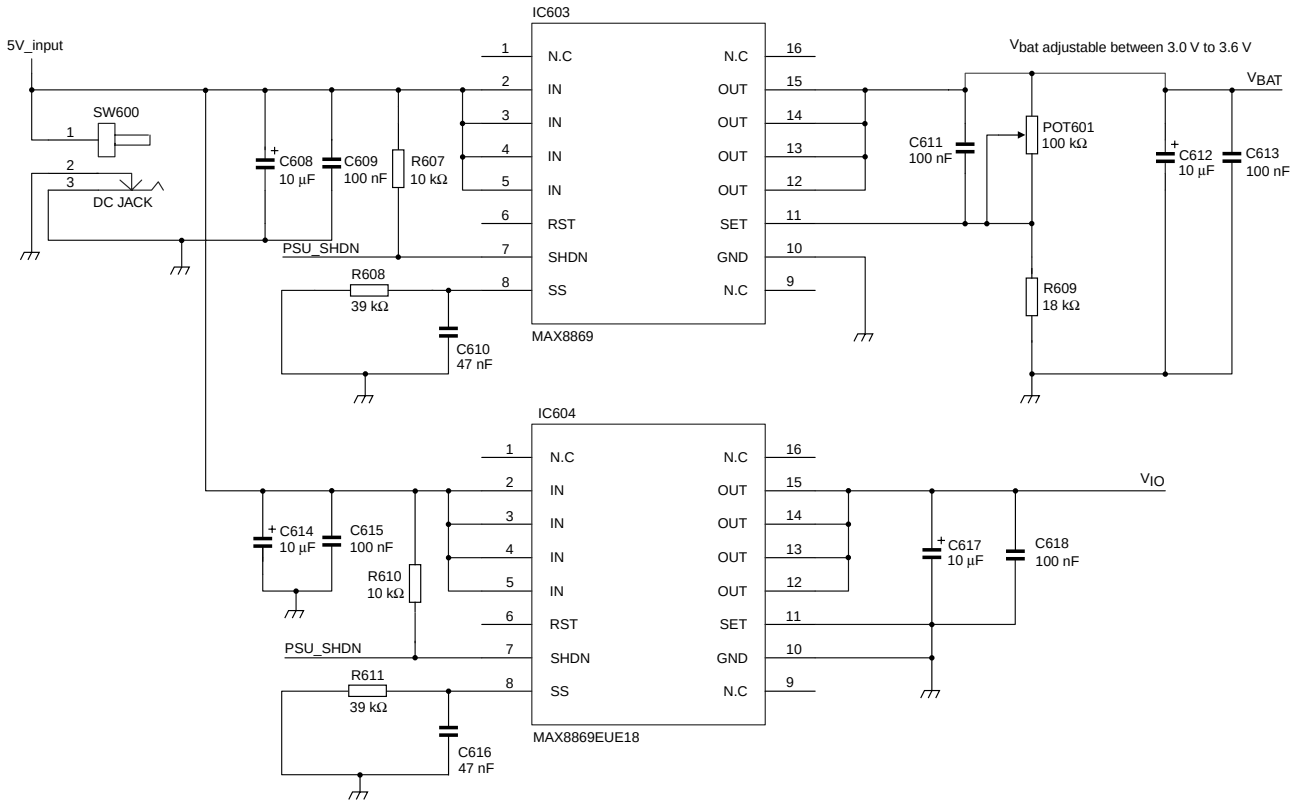

Fig 13. Schematics - 2

7. Components required when integrating

Table 2 provides the components that are required when integrating the ISP1506 into your design. For more information, refer to the ISP1506 data sheet.

Table 2. Components required when integrating the ISP1506

Designator	Component description	Location	Value	Remark
R600	Resistor for band gap reference	On RREF (pin 2)	12 kΩ ± 1 %	-
C600	Charge pump capacitor	Between C_B and C_A (pins 7 and 8)	270 nF	Capacitance determines the charge pump current
C601	Filter capacitor	On V_{BUS} (pin 10)	See Table 3	-
C602	Decoupling capacitor	On $V_{CC(3V3)}$ (pin 11)	100 nF	-
C603	Filtering capacitor	On $V_{CC(3V3)}$ (pin 11)	4.7 µF	-
Q601	Crystal oscillator	Between XTAL1 and XTAL2 (pins 12 and13)	ISP1506A: 19.2 MHz ± 50 ppm ISP1506B: 26 MHz ± 50 ppm	Not required if using clock from another source

Designator	Component description	Location	Value	Remark
			Remark: The ISP1506D is obsolete and the 12 MHz ± 50 ppm option is no longer available. **Remark**: Recommended crystal specification: Crystal drive level: 500 µW max; ESR ≤ 100 Ω max; shunt package capacitance = 7 pF max	
C604, C605	Load capacitor	Between XTAL1 and XTAL2 (pins 12 and13)	18 pF	Not required if using clock from another source
C606	Decoupling capacitor	On $V_{DD(1V8)}$ (pin 15)	100 nF	-
C607	Filter capacitor	On $V_{DD(1V8)}$ (pin 15)	4.7 µF	-
C620	Decoupling capacitor for $V_{CC(I/O)}$	On $V_{CC(I/O)}$ (pins 1, 21)	100 nF	-
C625	Decoupling capacitor for V_{BAT}	On V_{BAT} (pin 9)	100 nF	-
IC606	V_{BUS} power switch	Between PSW_N/RESET_N and V_{BUS}/FAULT	Any type of V_{BUS} power switch designed for USB application	Required only if the host is driving more than 50 mA
R613	Pull-up resistor	On PSW_N/RESET_N (pin 14)	10 kΩ	Required if V_{BUS} power switch is needed in the design

Table 3. Components Recommended V_{BUS} capacitor

These values are according to the Universal Serial Bus Specification Rev. 2.0 and On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a requirements.

CV_{BUS}	Min	Max	Unit
Host	120	-	µF
OTG	1	6.5	µF
Peripheral	1	10	µF

8. Bill of materials

Table 4. Bill of materials

Designator	Footprint	Comment
S600 S601 S602 S603 S604 S605 S606 S607 S608 S609 S610 S611 S612	SIP2-S	-
Q601	crystal	19.2 MHz
POT601	VARR	100 k
C619	CASE D	100 µF
C608 C612 C614 C617	ECASE-B	10 µF
C601 C603 C607	CASE B	4.7 µF
SW600	DC JACK	DC JACK
JP600 JP602	SIP3	Header 1x3
IC600	HVQFN24-SMT	ISP1506
IC601 IC602	IP4059CX5	IP4059CX/LF
IC603	TSSO5X6-G16	MAX8869
IC604	TSSO5X6-G16	MAX8869EUE18
IC605	SO-8	NDS9435A
IC606	SOP-8	MIC2026
IC607	TSSO5X6-G14/X.3	SN74LV14PWLE
CON600	USB_A	USB CON TYPE A
CON601	USB_B	USB CON TYPE B (optional)
CON602	USB_AB	USB Mini AB receptacle
JP601	2-557101-5	100PIN_T&MT
R601 R602 R603 R604 R605 R606 R618	0603	0 Ω
C602 C606 C609 C611 C613 C615 C618 C620 C621 C622 C623 C625 C626 C627 C628	0603	100 nF
R607 R610 R613 R614 R616	0603	10 kΩ
R600	0603	12 kΩ ± 1 %
R609	0603	18 kΩ
C604 C605	0603	18 pF
R615	0603	1K5
R612 R617 R619	0603	220 Ω

Designator	Footprint	Comment
C600	0603	270 nF
R608 R611	0603	39 kΩ
C610 C616	0603	47 nF
D600 D601	3mm_LED	LED

9. Abbreviations

Table 5. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
DDR	Double Data Rate
OTG	On-The-Go
T&MT	Transceiver and Macrocell Tester
ULPI	UTMI+ Low Pin Interface
UTMI	USB Transceiver Macrocell Interface
USB	Universal Serial Bus

10. References

- Universal Serial Bus Specification Rev. 2.0
- ISP1506 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet
- On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a
- UTMI+ Low Pin Interface (ULPI) Specification Rev 1.1
- USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver 1.2

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